Amendments to the Claims

Kindly amend claims 1, 7, 13 and 19; and cancel claims 2, 8, 14 and 20; as set forth below. In compliance with the Revised Amendment Format published in the Official Gazette on February 25, 2003, a complete listing of claims is provided herein. The changes in the amended claims are shown by strikethrough (for deleted matter) and underlining (for added matter).

1. (Currently Amended) A system for testing integrated circuitry comprising a plurality of clock domains and at least one integrated circuit chip, the system comprising:

a command transfer control hierarchy comprising a plurality of control levels, including a first level comprising a master command transfer control, and including at least one additional lower level, each lower level having a plurality of command transfer controls configured serially, each command transfer control of a last level being associated with at least one of the clock domains , the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines;

a communication protocol for communicating commands among the control levels; and

wherein command activation signals are immediately propagated serially from the first level to lower levels, and serially across command transfer controls in each level; and wherein command deactivation signals are communicated serially among and across control levels upon receipt of feedback from all lower levels that a commanded operation has been completed.

2. (Cancelled)

3. (Original) The system of claim 1, wherein the communication protocol comprises a global synchronization signal.

4. (Original) The system of claim 1, comprising an LBIST system.

5. (Original) The system of claim 4, wherein the command transfer control hierarchy controls the LBIST system such that LBIST testing is performed on the clock domains synchronously.

6. (Original) The system of claim 4, comprising a plurality of integrated circuit chips, wherein the command transfer control hierarchy controls the LBIST system such that LBIST testing is performed on the clock domains and across the chips synchronously.

7. (Currently Amended) A method for testing integrated circuitry comprising a plurality of clock domains and at least one integrated circuit chip, comprising:

providing a command transfer control hierarchy comprising a plurality of control levels, including a first level comprising a master command transfer control, and including at least one additional lower level, each lower level having a plurality of command transfer controls configured serially, each command transfer control of a last level being associated with at least one of the clock domains , the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines;

providing a communication protocol for communicating commands among the control levels; and

wherein command activation signals are immediately propagated serially from the first level to lower levels, and serially across command transfer controls in each level; and wherein command deactivation signals are communicated serially among and across control levels upon receipt of feedback from all lower levels that a commanded operation has been completed.

8. (Cancelled)

9. (Original) The method of claim 7, wherein the communication protocol comprises a global synchronization signal.

10. (Original) The method of claim 7, comprising an LBIST system.

11. (Original) The method of claim 10, wherein the command transfer control hierarchy controls the LBIST system such that LBIST testing is performed on the clock domains synchronously.

12. (Original) The method of claim 10, comprising a plurality of integrated circuit chips, wherein the command transfer control hierarchy controls the LBIST system such that LBIST testing is performed on the clock domains and across the chips synchronously.

13. (Currently Amended) An article of manufacture, comprising:

at least one computer usable medium having computer readable program code means embodied therein for effecting testing of integrated circuitry comprising a plurality of clock domains and at least one integrated circuit chip, the computer readable program code means in the article of manufacture comprising:

computer readable code means for providing a command transfer control hierarchy comprising a plurality of control levels, including a first level comprising a master command transfer control, and including at least one additional lower level, each lower level having a plurality of command transfer controls configured serially, each command transfer control of a last level being associated with at least one of the clock domains , the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines;

computer readable code means for providing a communication protocol for communicating commands among the control levels; and

wherein command activation signals are immediately propagated serially from the first level to lower levels, and serially across command transfer controls in each level; and wherein command deactivation signals are communicated serially among and across control levels upon receipt of

feedback from all lower levels that a commanded operation has been completed.

14. (Cancelled)

15. (Original) The article of manufacture of claim 13, wherein the communication protocol comprises a global synchronization signal.

16. (Original) The article of manufacture of claim 13, wherein the testing comprises LBIST.

17. (Original) The article of manufacture of claim 16, wherein the command transfer control hierarchy controls the LBIST testing such that testing is performed on all clock domains synchronously.

18. (Original) The article of manufacture of claim 16, comprising a plurality of integrated circuit chips, wherein the command transfer control hierarchy controls the LBIST testing such that testing is performed on the clock domains and across the chips synchronously.

19. (Currently Amended) At least one program storage device readable by a machine, tangibly embodying at least one program of instructions executable by the machine to perform a method for testing integrated circuitry comprising a plurality of clock domains, the method comprising:

providing a command transfer control hierarchy comprising a plurality of control levels, including a first level comprising a master command transfer control, and including at least one additional lower level, each lower level having a plurality of command transfer controls configured serially, each command transfer control of a last level being associated with at least one of the clock domains , the command transfer control hierarchy being scalable, the master command transfer control and each command transfer control each having an equal number of input lines and output lines;

providing a communication protocol for communicating commands among the control levels; and

wherein command activation signals are immediately propagated serially from the first level to lower levels, and serially across command transfer controls in each level; and wherein command deactivation signals are communicated serially among and across control levels upon receipt of feedback from all lower levels that a commanded operation has been completed.

20. (Cancelled)

21. (Original) The program storage device of claim 19, wherein the communication protocol comprises a global synchronization signal.

22. (Original) The program storage device of claim 19, wherein the method comprises LBIST.

23. (Original) The program storage device of claim 22, wherein the command transfer control hierarchy controls the LBIST method such that LBIST testing is performed on the clock domains synchronously.

24. (Original) The program storage device of claim 22, comprising a plurality of integrated circuit chips, wherein the command transfer control hierarchy controls the LBIST method such that LBIST testing is performed on the clock domains and across the chips synchronously.